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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,929	02/17/2004	Douglas J. Tweet	SLA 0735	1902
27518	7590	07/13/2005		EXAMINER LUU, CHUONG A
			ART UNIT 2818	PAPER NUMBER

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/780,929	TWEET ET AL.	
	Examiner Chuong A. Luu	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-13 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2/17/2004</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### PRIOR ART REJECTIONS

#### Statutory Basis

#### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

#### The Rejections

Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Maa et al. (U.S. 6,562,703 B1).

Maa a method for forming a relaxed SiGe layer with

**(1); (6); (9)** preparing a silicon substrate;

depositing a layer of SiGe to a thickness of between about 100 nm to 500 nm,

wherein the Ge content of the SiGe layer is equal to or greater than 10%;

implanting Ha+ ions through the SiGe layer into the substrate at a dose of between about 2x10<sup>14</sup> cm<sup>-2</sup> to 2x10<sup>16</sup> cm<sup>-2</sup> at an energy Of between about 20 kev to 100+ kev;

low temperature thermal annealing at a temperature of between about 200°C to 400°C for between about ten minutes and ten hours;

high temperature thermal annealing the substrate and SiGe layer, to relax the SiGe layer, in an inert atmosphere at a temperature of between about 650°C to 1000°C for between about 30 seconds and 30 minutes;

depositing a layer of tensile-stained silicon on the relaxed SiGe layer to a thickness of between about 5 nm to 30 nm (see column 3, lines 1-67, column 4, lines 1-67. Figures 1-6);

(2) wherein said depositing a layer of SiGe includes depositing the layer of SiGe at a temperature of between about 400°C to 600°C (see column 3, lines 1-67);

(3) which further includes, prior to said implanting, depositing a layer of silicon oxide on the SiGe layer to a thickness of between about 50Å to 300Å (see column 3, lines 1-67, column 4, lines 1-67);

(4) further includes, after said high temperature thermal annealing, depositing a layer of relaxed SiGe having a thickness of at least 100 nm on the relaxed SiGe layer (see column 3, lines 1-67, column 4, lines 1-67);

(5) wherein said low temperature thermal annealing is done in an inert atmosphere taken from the group of inert atmospheres consisting of argon and nitrogen (see column 3, lines 1-67, column 4, lines 1-67);

(7) further includes, prior to said implanting, depositing a layer of silicon oxide on the SiGe layer to a thickness of between about 50 Å to 300 Å (see column 3, lines 1-67, column 4, lines 1-67);

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(8) further includes, after said high temperature thermal annealing, depositing a layer of relaxed SiGe having a thickness of about 100nm on the relaxed SiGe layer (see column 3, lines 1-67, column 4, lines 1-67);

(10) further includes, prior to said implanting, depositing a layer of silicon oxide on the SiGe layer to a thickness of between about 50 Å to 300 Å (see column 3, lines 1-67, column 4, lines 1-67);

(11) wherein said high temperature thermal annealing is done in an inert atmosphere taken from the group of inert atmospheres consisting of argon and nitrogen (see column 3, lines 1-67, column 4, lines 1-67);

(12) which further includes, after said thermal annealing, depositing a layer of relaxed SiGe having a thickness of at least 100nm on the relaxed SiGe layer (see column 3, lines 1-67, column 4, lines 1-67);

(13) wherein said depositing a layer of silicon-based material on the relaxed SiGe layer includes depositing a layer of material taken from the group of materials consisting of tensile-stained silicon, tensile strained SiGe, compressed SiGe, and a composite stack thereof (see column 3, lines 1-67, column 4, lines 1-67. Figures 2-6).

## PRIOR ART REJECTIONS

### Statutory Basis

#### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### The Rejections

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mantl et al. (U.S. 6,464,780 B1).

Mantl discloses a monocrystalline substrate with

(1); (6); (9) preparing a silicon substrate;

depositing a layer of SiGe to a thickness of between about 2500 nm,

wherein the Ge content of the SiGe layer is equal to or greater than 10%;

implanting H<sub>a</sub><sup>+</sup> ions through the SiGe layer into the substrate at a dose of between about 2x10<sup>14</sup> cm<sup>-2</sup> to 2x10<sup>16</sup> cm<sup>-2</sup> at an energy Of between about 20 kev; low temperature thermal annealing at a temperature of between about 700°C for between about ten minutes and ten hours;

high temperature thermal annealing the substrate and SiGe layer, to relu the SiGe layer, in an inert atmosphere at a temperature of between about 1100°C for between about 30 seconds and 30 minutes;

depositing a layer of tensile-stained silicon on the relaxed SiGe layer to a thickness of between about 5 nm to 30 nm (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(2) wherein said depositing a layer of SiGe includes depositing the layer of SiGe at a temperature of between about 700°C (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(3) which further includes, prior to said implanting, depositing a layer of silicon oxide on the SiGe layer to a thickness of between about 50Å to 300Å (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(4) further includes, after said high temperature thermal annealing, depositing a layer of relaxed SiGe having a thickness of at least 100 nm on the relaxed SiGe layer (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(5) wherein said low temperature thermal annealing is done in an inert atmosphere taken from the group of inert atmospheres consisting of argon and nitrogen (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(7) further includes, prior to said implanting, depositing a layer of silicon oxide on the SiGe layer to a thickness of between about 50 Å to 300 Å (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(8) further includes, after said high temperature thermal annealing, depositing a layer of relaxed SiGe having a thickness of about 100nm on the relaxed SiGe layer (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(10) further includes, prior to said implanting, depositing a layer of silicon oxide on the SiGe layer to a thickness of between about 50 Å to 300 Å (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(11) wherein said high temperature thermal annealing is done in an inert atmosphere taken from the group of inert atmospheres consisting of argon and nitrogen (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(12) which further includes, after said thermal annealing, depositing a layer of relaxed SiGe having a thickness of at least 100nm on the relaxed SiGe layer (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2);

(13) wherein said depositing a layer of silicon-based material on the relaxed SiGe layer includes depositing a layer of material taken from the group of materials consisting of tensile-stained silicon, tensile strained SiGe, compressed SiGe, and a composite stack thereof (see column 3, lines 35-67 and column 4, lines 1-42. Figure 2).

Mantl teaches the outlined features above except for the thickness of the SiGe; the doping concentration, the energy level, the annealing temperature, time duration. However, the operational parameters, such as time and temperature and the thickness of the thin film are considered obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify such parameters of Mantl's device within the range as claimed for the purpose of providing for the suitable operational conditions to obtain the semiconductor device with the maximum speed, and it also has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP j 2144.05).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong Anh Luu  
Patent Examiner  
June 6, 2005